

Abstract of the Disclosure

The output of each cell in an A-D converter on an IC chip is dependent upon the relative values of an input voltage and an individual one of progressive fractions of a reference voltage respectively introduced to the branches in a differential amplifier. To minimize output errors from cell mismatches, first and second sets of averaging impedances, preferably resistors, are respectively connected between the output terminals in the first branches, and the output terminals in the second branches, in successive pairs of cells. The impedances have relatively low values, particularly compared to the impedances of current sources connected to the branch output terminals. First and second resistive strips on the chip may be tapped at progressive positions to respectively define the impedances in the first and second sets. One end of each strip may be connected to the opposite end of the other strip to define a closed impedance loop for minimizing averaging errors at the strip ends. Different fractions of the reference voltage are associated with each individual impedance in the first and second sets. Such reference voltage fractions have a particular repetitive relationship. In this way, the number of output terminals is reduced and cell mismatches are reduced. The different outputs at each individual impedance are determined for the progressive fractions of the reference voltage at such impedance. Successive voltage fractions for each impedance have opposite polarities to provide a folding relationship. Such outputs may be cascaded to further reduce cell mismatches and the number of output terminals.

This invention relates to integrated circuits in which repetitive cells are matched for optimal circuit operation. More particularly, this invention relates to integrated circuits in

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which the effects of any cell mismatches are minimized. The invention is particularly adapted to be used in analog-to-digital converters. The invention additionally relates to methods of minimizing the effects of cell mismatches on cell  
5 outputs.

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